Columbia University
Department of Electrical Engineering
Solid State Devices and Materials
ELEN E3106/4106
Homework #8

Due: Friday, November 21st by 5pm
Goal: Practice solving practical problems in MOS capacitors. Gain an intuitive understanding of the basic device operation under various gate biasing conditions. Practice drawing energy band and charge diagrams.
Instructions: Show your work and include units in answers for full credit. Unless stated otherwise, make the assumptions we have been taking in class (the sample is at 300 K) Circle or box your final answer. Assume $\epsilon_{SiO_2} = 3.9\epsilon_0$ and $\chi_{Si} = 4.05\ V$ for Si, p+ poly-Si, and n+ poly-Si.
Points: 110 pts for 3106. 130 pts for 4106.

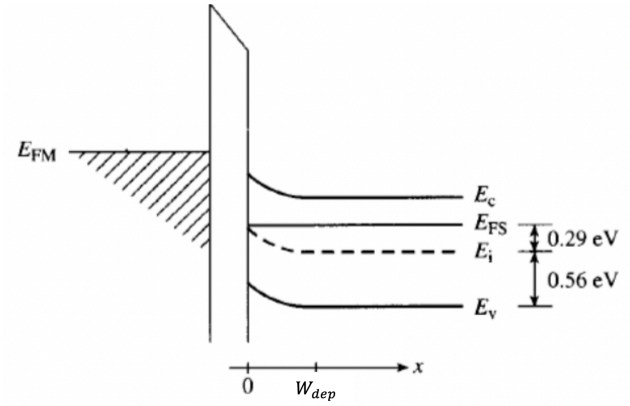
- **Problem 1 (20 pts)** MOS fundamentals.

Consider an ideal MOS capacitor fabricated on a p-type silicon with a doping of $N_a = 6 \times 10^{16}\ cm^{-3}$ with an oxide thickness of 3 nm and an n+ poly-gate.

(a) What is the flat-band voltage, V_{fb}, of this capacitor?
(b) Calculate the maximum depletion region width, W_{dmax}.
(c) Find the threshold voltage, V_t, of this device.
(d) If the gate is changed to p+ poly, what would the threshold voltage be now?

- **Problem 2 (32 pts)** MOS fundamentals.

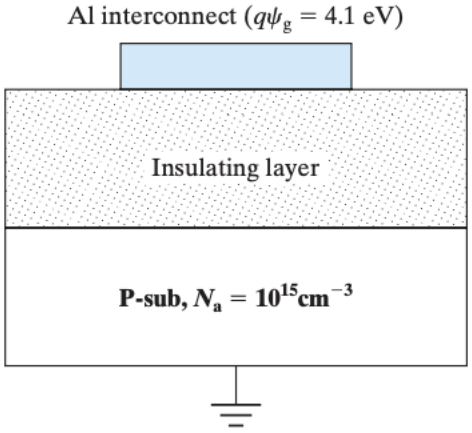
The energy band diagram for an MOS capacitor with insulator thickness 10 nm is sketched in the figure below. The Si substrate is grounded and a voltage V_g is applied to the metal gate. Please assume room temperature and otherwise an ideal capacitor (no trapped oxide charges) in answering the questions below.



(a) Is this device NMOS or PMOS? Explain.
(b) Is the device in accumulation, flat-band, depletion, threshold, or inversion? How can you tell?

(c) Sketch the potential $\Phi(x)$ as a function of position along the entire structure. (Hint: recall potential energy follows the negative trend of the energy bands).
(d) Sketch the electric field $E(x)$ as a function of position along the entire structure. (Hint: recall the electric field is the negative slope of potential).
(e) What is the electron concentration at the Si-SiO_2 interface (Hint: notice $E_{Fs} = E_i$ at the interface. What do we know about the concentration at E_i?).
(f) What is the bulk Si doping, N_d?
(g) What is the voltage drop across the oxide, V_{ox}?
(h) What is the applied gate voltage if we let $\Phi_M = \Phi_{semi}$?

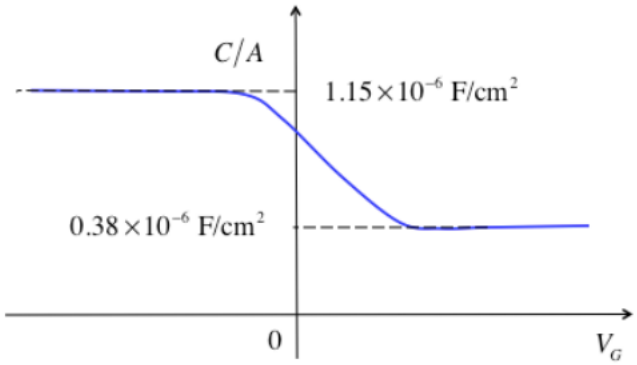
- **Problem 3 (28 pts)** Application: designing metal interconnects in IC circuits.
Metal interconnect lines in IC circuits form parasitic MOS capacitors as illustrated in the figure below. Generally, one wants to prevent the underlying Si substrate from becoming inverted. Otherwise, parasitic transistors may be formed and create undesirable current paths between the n+ diffusions. (Note: $q\psi_g = q\Phi_M$ is the work function of the metal interconnect acting as the gate).



(a) Find V_{fb} of this parasitic MOS capacitor.
(b) If the interconnect voltage can be as high as 5 V, what is the maximum capacitance (in F/cm^2) of the insulating layer that can be tolerated without forming an inversion layer?
(c) If the insulating layer thickness must be 1 μm for fabrication considerations, what should the dielectric constant ($K = \epsilon/\epsilon_0$) of the insulating material be to make V_t = 5 V?
(d) Is the answer in (c) the minimum or maximum allowable K to prevent inversion?
(e) At $V_g = V_t + 2\,V\,(V_t = 5\,V)$, what is the area charge density (C/cm^2) in the inversion layer?
(f) At $V_g = V_t = 5\,V$, what is the high-frequency MOS capacitance (in F/cm^2)?
(g) At $V_g = V_t + 2\,V\,(V_t = 5\,V)$, what voltage is dropped across the insulating layer?

- **Problem 4 (10 pts)** MOS C-V characteristics.

A high-frequency MOS capacitance vs. voltage curve is shown below. Answer the following questions assuming that the semiconductor is silicon at room temperature.



(a) Is the semiconductor n-type or p-type? Explain your answer.
(b) What is the thickness of the oxide?
(c) What is the thickness of the depletion layer in inversion? (Hint: You will need to find the depletion capacitance first).
(d) Explain how you could calculate the doping density of the semiconductor.

- **Problem 5 (20 pts)** Band bending in the semiconductor of an MOS capacitor.

In an MOS capacitor, the bandbending in the semiconductor is of paramount importance. If Φ_s is the potential at the surface, and $\Phi = 0$ is the potential in the bulk, then $-q\Phi_s$ is the total bandbending in the semiconductor. A negative Φ_s means the bands bend up, and a positive Φ_s means the bands bend down. This question helps familiarize you with surface potential and bandbending. Assume a Si MOS capacitor at room temperature.

(a) Assume $N_a = 10^{17}\ cm^{-3}$ compute $\Phi_B = (E_i - E_F)/q$, which plays an important role in MOS electrostatics.
(b) Assume $\Phi_s = \Phi_B$ and sketch the energy band diagram and the charge density, $\rho(x)$ vs. position in the semiconductor.
(c) Assume $\Phi_s = -\Phi_B$ and sketch the energy band diagram and the charge density, $\rho(x)$ vs. position in the semiconductor.
(d) Assume $\Phi_s = 0$ and sketch the energy band diagram and the charge density, $\rho(x)$ vs. position in the semiconductor.
(e) Assume $\Phi_s = 2\Phi_B$ and sketch the energy band diagram and the charge density, $\rho(x)$ vs. position in the semiconductor.

- **Problem 6 (20 pts) (Required for 4106 students ONLY, 20 pts)** Flash memory cell.

A Flash memory cell stores electronic charge on a "floating gate" isolated by SiO_2 from the top control gate and the silicon substrate. The trapped charge Q is written and erased by high-field tunneling through the bottom "tunnel oxide." The presence or absence of Q shifts the threshold voltage V_t, which can be externally read by the control gate. Consider a Flash cell with dimensions

$L \times W = 30\ x\ 60\ nm$, and assume both oxide layers as well as the floating gate are 10 nm thick. The control and floating gates are n+ polysilicon and the p-doped substrate is $10^{18}\ cm^{-3}$.

(a) If a threshold voltage shift $\Delta V_t = 2\ V$ is sufficient to distinguish between a "0" and a "1", how much charge Q must be stored on the floating gate? You may assume that Q is uniformly distributed in the floating gate, both in the vertical and lateral directions.

(b) How many electrons are stored on the floating gate in the charged "0" state?

(c) The state of the bits (for example, your music collection) must be preserved for 10 years, and over this period of time ΔV_t should not drop by more than 20%. What is the maximum allowed leakage current in electrons per month?